CLOCK SIGNAL SELECTOR CIRCUIT WITH REDUCED PROBABILITY OF ERRONEOUS OUTPUT DUE TO METASTABILITY

ABSTRACT OF THE DISCLOSURE

A clock signal selector circuit is disclosed including a synchronizer circuit, two switching circuits, and a multiplexer. The synchronizer circuit synchronizes a first control signal to a first clock signal, thereby producing a second control signal. A first switching circuit produces the first clock signal at a first node when the second control signal is asserted. The multiplexer drives a second node with a signal at the first node when the second control signal is asserted. The second switching circuit forms an electrical connection between the first and second nodes when the second control signal is deasserted. The two switching circuits significantly reduce a probability of error at the second node due to metastability when the second control signal transitions from asserted to deasserted and the first clock signal is deselected. The second switching circuit provides electrical feedback from the second node to the first node.